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IN THE SPECIFICATION

Please replace paragraph [40] with the following paragraph:

For every ultrasound beam, the cache memory and controller 112 connects over digital signal lines ~~132~~ 133 (e.g., carried by a separate flex cable) to each signal processor controller which may be included within memory 108 on each processing board 106. The signal processor controller which may be included within memory 108 are drawn as a separate block labeled 'memory' on the processing board 106, but may also be included as part of the signal processor 110. The cache memory and controller 112 transfers static and dynamic probe setup information to the signal processor 110. Static setup information is typically spatial element locations, power settings, and delay setting mapping tables. Dynamic information is typically directional information for the sub-apertures that vary from beam to beam. The digital signal lines may include, for example, a clock line for each processing board 106, a serial command data line for each processing board 106, one or more data lines connected to each processing board 106, an output enable for one or more of the signal processors 110, and a test signal.

Please replace paragraph [43] with the following paragraph:

[0043] In one implementation, the cache memory in the cache memory and controller ~~132~~ 112 is organized into of 512k words x 16 bit (8 Mbit) and divided into pages of 128 words. The cache memory pointer can be set to the start of each page. The cache memory pointer may be, for example, a 12 bit pointer that may address a total of 4096 pages. When the cache memory 132 is a 4 Mbit cache, the cache memory pointer may be an 11 bit pointer to index 2048 pages. The words of a cache page are employed when writing or reading data to or from a chain of signal

processors 110. The digital data lines for the signal processors 110 on each processing board may be chained through shift registers over a series of plural signal processors 110. Thus, data transferred to the signal processors 110 propagates serially through the signal processors 110. The bit from the word with the lowest address in a page will end in the LSB bit of the shift register to the last signal processor 110 in a chain when loading data. Further, the cache memory 132 is shown within the cache memory and controller 112, but in alternate implementations the cache memory 132 may be separate from the cache memory and controller 112. The cache memory may also be part of the signal processors 110.

Please replace paragraph [60] with the following paragraph:

[0060] When the probe 100 is connected to the host system 116, the host system 116 transfers the setup information for each aperture and each beam into the SRAM on the location memory controller 112. The receive beamforming is split between the host system 116 and the probe ~~104~~100. The host system 116 is responsible for the beamforming delay, aperture expansion, and amplitude apodization of the system receive channels driven by the signal processors 110 on the receive aperture outputs.

Please replace paragraph [97] with the following paragraph:

[0097] The circuitry in the signal processor 110 is described in more detail below with regard to Figure 10. Figure 10 shows the narrowband beamforming circuitry 1000 in the signal processor 110. Each receive input (one of which is labeled sxIn0) passes through a low-noise amplifier 1002, a weighting and summation stage including mixers (one of which is labeled 1004), summers (a positive summation summer labeled 1005 and a negative summation summer labeled 1006),

and all-pass filters 1008 and 1009. ~~in~~ In addition the all-pass filters connect to second summers (one of which is labeled 1010) and through a line driver 1012 out to the receive sub-aperture output (one of which is labeled sxOut).

Please replace paragraph [102] with the following paragraph:

[00102] The summation stage 1010, having the second summers, may further include an attenuation to level the signal swing of the available range.